RCC700A

Fibre Channel Transceiver

240 to 330 Megabaud

Features

- 240 to 330 Megabaud data rates
- Compliant with Fibre Channel standard
- Submicron CMOS technology
- PLL clock and data recovery
- Clock synthesizer
- Selectable 8 bit/10 bit encode, 10 bit/8 bit decode
- Parity generate/check
- Low power dissipation: 600 mW typ. at 250 Megabaud
- Byte sync on K28.1, K28.5 or K28.7
- Single power supply: +5V
- CMOS/TTL compatible parallel data inputs/outputs
- PECL compatible serial data inputs/outputs
- Available in 64-pin PQFP, 68 pin PLCC

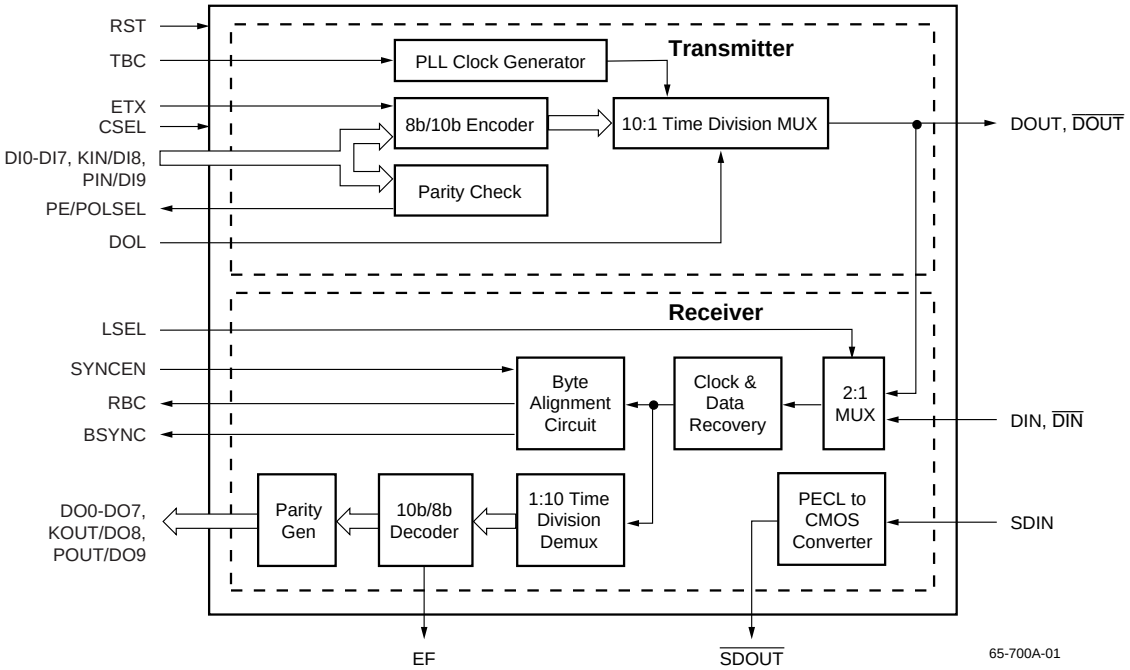
Applications

- Fibre Channel Transceiver
- High-speed Fiber Optics or Copper links
- High-resolution graphic display terminal
- LAN Switching
- Video data transmission

Description

The RCC700A is a monolithic transmitter/receiver IC integrating a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a phase-locked loop clock synthesizer, a 10:1 mux, a 1:10 demux, an 8-bit/10-bit encoder, and an 10-bit/8-bit decoder. It operates with a single +5V power supply. The RCC700A provides a complete physical interface in compliance with the Fibre Channel Physical Layer Standard (FC-PH) specifications at 265.625 Megabaud (Mbaud). 8 bit/10 bit encoder and 10 bit/8 bit decoder can be disabled through an external pin.

Block Diagram



Functional Description

Transmitter Section

The RCC700A transmitter section includes a phase-locked loop synthesizer, an 8-bit/10-bit encoder, an input parity checker and a 10:1 multiplexer. The RCC700A accepts a CMOS/TTL data byte (DI0-DI7) along with the K character indicator (KIN) and parity bit (PIN) for CSEL = 0. For CSEL = 1, KIN and PIN become DI8 and DI9, respectively.

The Parity Check circuitry calculates the odd parity of the input data byte and compares it with PIN. If the calculated parity differs from PIN, the transmitter flags the error by bringing the parity error bit, PE to a HIGH level. For example, for DI0-DI7=00000101, PIN should be 1. If PIN is not equal to 1, PE=1.

The RCC700A transmitter section encodes the CMOS/TTL input data bye (DI0-DI7) into a 10-bit word using IBM's 8-bit/10-bit coding (see Table 2). The encoder is disabled if CSEL = 1, and enabled if CSEL = 0. The encoded word is then converted to a serial high speed data stream (DOUT/$\overline{\text{DOUT}}$) at 240 to 330 Mbaud via a 10:1 time division mux. The serial data stream (DOUT/$\overline{\text{DOUT}}$) is transmitted at PECL levels (positive shifted ECL levels, Vth = +3.4V).

The RCC700A features a Data Output Low function (DOL) that can force the data output (DOUT, $\overline{\text{DOUT}}$) to logic LOW for protection of the fiber optic module transmitter diode. DOL is controlled by the Protocol IC or the fiber optic transmitter module. The RCC700A also incorporates an Error Transmit input (ETX). The RCC700A sends a violating code when ETX is brought to a logic HIGH. If ETX stays HIGH for more than one byte clock cycle, the transmitter will send error bytes of alternate running disparities in order to maintain the DC balance of the line (100111 1011 or 011000 0100).

The 240 to 330 MHz clock used for the serial stream is generated using a PLL clock generator which multiplies the input frequency, 24 to 33 MHz, by a factor of 10. The input clock reference for the PLL clock generator, Transmit Byte Clock (TBC), typically comes from a crystal oscillator or from the system.

Receiver Section

The RCC700A receiver section includes a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a byte alignment circuit, a 1:10 demultiplexer, an 10-bit/8-bit decoder, a disparity/code violation checker and a parity generator. The RCC700A accepts a differential data stream (DIN/$\overline{\text{DIN}}$) at 240 to 330 Mbaud, recovers the clock and regenerates the encoded serial data. The recovered encoded data is then converted to 10 parallel data lines via a 1:10 time division demultiplexer and decoded into an 8-bit byte via the 10-bit/8-bit decoder. The decoder is disabled if CSEL = 1, and enabled if CSEL = 0. K Command characters are also detected and indicated by bringing the KOUT pin to a HIGH level. The odd parity of the output 8-bit byte (DO0-DO7) is calculated and available at pin POUT. For example, for DO0-DO7=00000101, POUT should be 1. For CSEL = 1, KOUT and POUT become D08 and D09, respectively. The RCC700A also generates a Receive Byte Clock (RBC) for driving the CMOS protocol layer IC. All the outputs to the protocol layer IC are at CMOS levels.

Running disparity and coding is checked during the 10-bit/8-bit decoding and violations are flagged by bringing the Error Flag (EF) to a HIGH level. If consecutive bytes have more 1s or more 0s, or if running disparity is different from expected for the received code, or the transmission character is not part of Table 2, EF goes HIGH. If 100111 1011 or 011000 0100 is received, EF=1, KOUT=1, DO0-DO7=00000000.

The RCC700A contains a byte synchronization circuitry. When enabled (SYNCEN HIGH), the RCC700A will automatically resynchronize the demultiplexer to byte align with the leading seven bits (00111 11 or 11000 00) of the transmission character, corresponding to reception of K28.1, K28.5 or K28.7.

SYNCEN pin gives the protocol layer IC the flexibility to request the RCC700A to align only when required, e.g. at power up or after loss of byte synchronization. The RCC700A also incorporates a PECL to CMOS converter to translate the PECL output signal from an optical receiver module SDIN to a CMOS output signal. This allows for direct interfacing with the CMOS protocol layer circuit. SDIN is active HIGH. Therefore, $\overline{\text{SDOUT}}$ will be at a CMOS level LOW when an optical signal is present at the input of the fiber optics receiver module.

Loopback Test Mode

The RCC700A features an internal differential loopback for on-board diagnostic of the device. When loop select (LSEL) is HIGH, the receiver accepts the output data from the transmitter section (DOUT, $\overline{\text{DOUT}}$). When LSEL is LOW, i.e., tied to GND, the receiver accepts the incoming input data (DIN, $\overline{\text{DIN}}$).

Use of Table 2 for Encoding/ Decoding

The following information describes how Table 2 can be used for generating valid transmission characters (encoding) and checking the validity of received transmission characters (decoding).

The transmission character is labelled "abcdeifghj". The transmission order is a,b,c...j in that order. HGFEDCBA cor-

responds to the data inputs DI7...DI0 in that order. In the table, each valid data byte and special code byte has two columns corresponding to the current value of the running disparity (CURRENT RD- or CURRENT RD+). Running disparity is a binary parameter with either the value + or -.

The transmitter calculates the new running disparity based on the contents of the transmitted character. Similarly, the receiver calculates the new running disparity based on the contents of the received character.

The first six bits of the character, "abcdei," form one sub-block, and "fghj" forms another sub-block for computing running disparity. Running disparity (CURRENT RD+ or CURRENT RD-) at the beginning of the 6-bit sub-block is the running disparity at the end of the last transmission character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the transmission character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-block is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block if 0011.

2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100.

3. If neither of the above two conditions applies, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

CURRENT RD is used to select the transmission character for the data byte or special code.

While decoding the received character, the column corresponding to the current value of the receiver's running disparity shall be searched for the received transmission character. If the received transmission character is found in the proper column, the transmission character is considered valid and the associated data or special code byte decoded. Otherwise, the character is considered invalid and EF pin is held HIGH for that byte. Independent of the transmission character's validity, the received transmission character shall be used to calculate a new value of running disparity.

Detection of code violation (EF=HIGH) does not necessarily indicate that the transmission character in which the code violation was detected is in error. Code violation may occur due to the prior error which altered the running disparity of the bit stream but did not result in a detectable error at the transmission character in which it occurred. An example of an error scenario where the error is flagged after it happens is shown below (see Table 1).

Reset Function

For CSEL = 0, during normal operation, the reset input pin, RST, is LOW and is not used. Under total failure of receive PLL to acquire lock, this reset function can be used. When RST goes HIGH for at least 1 byte clock, the chip is reset, i.e. the receive PLL acquires lock to the bit clock derived from the TBC reference byte frequency and then to the incoming data.

For CSEL = 1, RST is normally HIGH and is LOW for at least 1 byte clock to reset.

Table 1. Example of Error Scenario

	RD	Character	RD	Character	RD	Character	RD
Transmitted character stream	-	D21.1	-	D10.2	-	D23.5	+
Transmitted bit stream	-	101010 1001	-	010101 0101	-	111010 1010	+
Bit stream after error	-	101010 1011	+	010101 0101	+	111010 1010	+
Decoded character stream	-	D21.0	+	D10.2	+	Error	+

Table 2. 8b/10b Encoding

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.3	010	11111	101011	0101	010100	0101

Table 2. 8b/10b Encoding (continued)

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.5	100	00110	011001	1101	011001	0010
D7.5	100	00111	111000	1101	000111	0010
D8.5	100	01000	111001	0010	000110	1101
D9.5	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Table 2. 8b/10b Encoding (continued)

DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA	abcdei	fghj[2]	abcdei	fghj[2]
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110

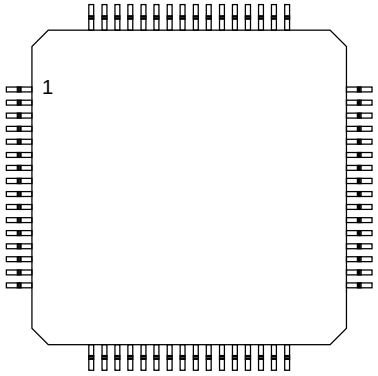
DATA[3] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA	abcdei	fghj[2]	abcdei	fghj[2]
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

DATA[4] BYTE NAME	BITS		CURRENT RD-		CURRENT RD+	
	HGF	EDCBA[1]	abcdei	fghj[2]	abcdei	fghj[2]
K28.0	000	11100	001111	0100	110000	1011
K28.1	001	11100	001111	1001	110000	0110
K28.2	010	11100	001111	0101	110000	1010
K28.3	011	11100	001111	0011	110000	1100
K28.4	100	11100	001111	0010	110000	1101
K28.5	101	11100	001111	1010	110000	0101
K28.6	110	11100	001111	0110	110000	1001
K28.7	111	11100	001111	1000	110000	0111
K23.7	111	10111	111010	1000	000101	0111
K27.7	111	11011	110110	1000	001001	0111
K29.7	111	11101	101110	1000	010001	0111
K30.7	111	11110	011110	1000	100001	0111

Notes:

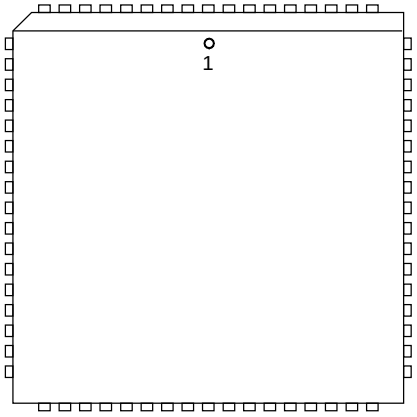
1. "HGF EDC BA" corresponds to DI7 ...0 in that order
2. a is to be transmitted first, followed by b, c, d ....j in that order
3. Kin=0
4. Kin=1

Pin Assignments



65-700A-02

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DO2	17	DI7	33	DOUT	49	$\overline{\text{SDOUT}}$
2	DO1	18	DI6	34	$\overline{\text{DOUT}}$	50	CSEL
3	DO0	19	DI5	35	LSEL	51	SYNCEN
4	DVCC	20	DI4	36	AGND	52	BSYNC
5	DVCC	21	DI3	37	AVCC	53	DVCC
6	DGND	22	DI2	38	AVCC	54	DGND
7	DGND	23	DI1	39	AGND	55	DVCC
8	POUT/DO9	24	DI0	40	AGND	56	DGND
9	KOUT/DO8	25	DGND	41	AVCC	57	DVCC
10	EF	26	TBC	42	AVCC	58	DGND
11	RBC	27	DVCC	43	AGND	59	DO7
12	DGND	28	RST	44	AVCC	60	DO6
13	PE/POLSEL	29	DGND	45	AGND	61	DO5
14	PIN/DI9	30	DVCC	46	SDIN	62	DO4
15	KIN/DI8	31	DOL	47	$\overline{\text{DIN}}$	63	D03
16	ETX	32	DGND	48	DIN	64	DGND



65-700A-07

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DGND	18	POUT/DO9	35	DI0	52	AGND
2	DVCC	19	KOUT/DO8	36	DGND	53	AVCC
3	DGND	20	EF	37	TBC	54	AVCC
4	DO7	21	RBC	38	DVCC	55	AGND
5	DO6	22	DGND	39	RST	56	AVCC
6	DO5	23	PE/POLSEL	40	DGND	57	AGND
7	DO4	24	PIN/DI9	41	DVCC	58	SDIN
8	DO3	25	KIN/DI8	42	DOL	59	$\overline{\text{DIN}}$
9	DGND	26	ETX	43	DGND	60	DIN
10	DGND	27	DGND	44	DOUT	61	DGND
11	DO2	28	DI7	45	$\overline{\text{DOUT}}$	62	$\overline{\text{SDOUT}}$
12	DO1	29	DI6	46	NC	63	CSEL
13	DO0	30	DI5	47	LSEL	64	SYNCEN
14	DVCC	31	DI4	48	AGND	65	BSYNC
15	DVCC	32	DI3	49	AVCC	66	DVCC
16	DGND	33	DI2	50	AVCC	67	DGND
17	DGND	34	DI1	51	AGND	68	DVCC

Pin Descriptions

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
DVCC	4, 5, 27, 30, 53, 55, 57	2, 14, 15, 38, 41, 66, 68	Positive supply for digital circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
AVCC	37, 38, 41, 42, 44	49, 50, 53, 54, 56	Positive supply for analog circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
DGND	6, 7, 12, 25, 29, 32, 54, 56, 58, 64	1, 3, 9, 10, 16, 17, 22, 27, 36, 40, 43, 61, 67	Chip ground for digital circuitry. DGND should be connected to the printed circuit board's ground plane at the pins.
AGND	36, 39, 40, 43, 45	48, 51, 52, 55, 57	Chip ground for analog circuitry. AGND should be connected to the printed circuit board's ground plane at the pins.
DI0-DI7	24, 23, 22, 21, 20, 19, 18, 17	35, 34, 33, 32, 31, 30, 29, 28	Transmitter input data (TTL levels).

Pin Descriptions (continued)

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
TBC	26	37	Transmit Byte Clock input (TTL level). Input reference frequency for the internal high speed clock generator: 24 to 33 MHz.
KIN/DI8	15	25	K character indicator input/Transmitter input data (TTL levels). If CSEL = 0, this pin in KIN. If CSEL = 1, this pin is DI8.
PIN/DI9	14	24	Odd parity input /Transmitter input data (TTL levels). If CSEL = 0, this pin in PIN. If CSEL = 1, this pin is DI9.
PE/ POLSEL	13	23	Parity Error indicator output/Polarity Select Input (CMOS/TTL levels). For CSEL = 0, This pin is PE. For CSEL = 1, This pin is POLSEL. PE will stay low when the on-chip calculated odd parity matches the incoming parity PIN. If there is a parity error, the PE flag is raised to a level HIGH. If POLSEL = 0, the receive data output timing specifications are with respect to the positive edge of RBC. If POLSEL = 1, the above specifications are with respect to the negative edge of RBC.
DOUT/ $\overline{\text{DOUT}}$	33,34	44,45	Transmitter differential output data (PECL levels). The output is a current mode driver with a nominal current driver of 8 mA. To generate a 0.8 V swing, use a 100Ω resistor across DOUT, $\overline{\text{DOUT}}$.
DOL	31	42	Data Output Low control input (TTL level). When HIGH, it forces the output to a logic low state (DOUT = LOW and $\overline{\text{DOUT}}$ = HIGH) to protect the fiber optic source. Connect to GND or leave open when not used.
LSEL	35	47	Loop Select input (TTL level). Internal differential loopback for "on-board" diagnostic of the device. When loop select (LSEL) is HIGH, the receiver accepts the output data from the transmitter section (DOUT/$\overline{\text{DOUT}}$). When LSEL is LOW, i.e. tied to GND, the receiver accepts the incoming input data (DIN/$\overline{\text{DIN}}$). Connect to GND or leave open when not used.
DIN/$\overline{\text{DIN}}$	48, 47	60, 59	Receiver differential input data (PECL levels).
SYNCEN	51	64	Byte Synchronization Enable input (TTL level). When SYNCEN is HIGH, the RCC700A will automatically resynchronize the demultiplexer to byte align with the received K28.1, K28.5 or K28.7 for both negative and positive running disparities (RD- and RD+). Connect to GND or leave open when not used.
BSYNC	52	65	Byte Synchronized output flag (CMOS levels). BSYNC goes to a HIGH level for one byte clock when SYNCEN is HIGH and the RCC700A detects and resynchronizes on K28.1, K28.5 or K28.7.
SDIN	46	58	Signal Detect input (PECL level). PECL input of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. Leave open when not used.
$\overline{\text{SDOUT}}$	49	62	Signal Detect Output (CMOS level). CMOS output of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. $\overline{\text{SDOUT}}$ is LOW when SDIN is HIGH.
DO0-DO7	3, 2, 1, 63, 62, 61, 60, 59	13, 12, 11, 8, 7, 6, 5, 4	Receiver output data/Receive output data (CMOS levels).
KOUT/DO8	9	19	K character indicator output / Receive Output Data (CMOS level). If CSEL = 0, this pin is KOUT. If CSEL = 1, this pin is DO8.
POUT/DO9	8	18	Odd parity output/Receive output data (CMOS level). If CSEL = 0, this pin is POUT. POUT is HIGH when the parity of the DO0...DO7 byte is even. If CSEL = 1, this pin is DO9.

Pin Descriptions (continued)

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
RBC	11	21	Receive Byte Clock output (CMOS level): 24 to 33 MHz.
EF	10	20	Error Flag output (CMOS level). EF goes HIGH to flag running disparity and coding violations detected during the 10b/8b decoding.
RST	28	39	Asynchronous reset input (TTL level). For CSEL = 0, this pin is normally LOW, and when HIGH for at least one byte clock, is used to reset all functions of the chip. This is a master reset. For CSEL = 1, this pin is normally HIGH, and when LOW for at least one byte clock, provides reset.
ETX	16	26	Error Transmit input (TTL level). This pin is only applicable of CSEL = 0 and is a No Connect for CSEL = 1. This pin is normally LOW. This pin, when HIGH, is used to force DC balanced alternating violation codes on its serial output.
CSEL	50	63	Select input (TTL level). This pin is normally low and enables the 8b/10b encoder/decoder circuitry. When high, the 8b/10b encoder/decoder is disabled and the following pins are affected: PIN/DI9, KIN/DI8, POUT/DO9, KOUT/DO8, PE/POLSEL, RST, and ETX.
NC	—	46	No connection.

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
Storage temperature range	-65	150	°C
Junction temperature range	-55	150	°C
Lead temperature range (soldering, 10 seconds)		300	°C
Positive power supply, V_{CC}	0	6	V
Voltage applied to any TTL inputs	-1	6	V
Voltage applied to any CMOS inputs	-1	6	V
Voltage applied to any PECL inputs	-1	6	V
Voltage applied to any CMOS outputs	-1	6	V
Voltage applied to any PECL outputs	-1	6	V
Current from any CMOS outputs	-50	50	mA
Current from any PECL outputs	-50	50	mA

Note:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_A	Ambient operating temperature	0		70	°C
V_{CC}	Positive supply voltage (DVCC and AVCC)	4.75	5.0	5.25	V
R_I	PECL differential load resistance[1]	80	100	150	Ω

Note:

1. Differential load resistance of 100Ω equals connection of 50Ω to AC ground on each of DOUT, $\overline{DOUT}$.

DC Electrical Characteristics

V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Transmitter						
V_{IH}	TTL input voltage HIGH		2.0		V_{CC} +0.5	V
V_{IL}	TTL input voltage LOW				0.8	V
I_{IH}	TTL input HIGH current	V_{CC} = max, V_{IN} = 2.7V			100	µA
I_{IL}	TTL input LOW current	V_{CC} = max, V_{IN} = 0.4V	-1		100	µA
C_I	Input capacitance			4	10	pF
V_{OHP}	PECL output voltage HIGH	R_{DIFF} = 100Ω, V_{CC} = 5V	3.5	3.8	4.2	V
V_{OLP}	PECL ouput voltage LOW	R_{DIFF} = 100Ω, V_{CC} = 5V	2.6	3.0	3.4	V
V_{OP}	PECL output voltage amplitude	V_{OHP} - V_{OLP}, V_{CC} = 5V	0.6	0.8	1.0	V
I_O	PECL output current			8		mA
Receiver						
V_{IH}	TTL input voltage HIGH		2.0		V_{CC} +0.5	V
V_{IL}	TTL input voltage LOW		0		0.8	V
I_{IH}	TTL input HIGH current	V_{CC} = max, Vin = 2.7V			100	µA
I_{IL}	TTL input LOW current	V_{CC} = max, Vin = 0.4V			-100	µA
V_{CM}	Com. mode range (DIN, $\overline{DIN}$)		2.8		4.5	V
V_{DIFF}	Diff. input voltage (DIN, $\overline{DIN}$)		0.4			V
I_{IPH}	PECL input HIGH current	V_{IH} = V_{CC} -0.88V			100	µA
I_{IPL}	PECL input LOW current	V_{IL} = V_{CC} - 1.81V	-100			µA
V_{OHC}	CMOS output voltage HIGH	I_{OH}= -4.1mA (-8.1mA for RBC)	3.5		V_{CC}	V
V_{OLC}	CMOS output voltage LOW	I_{OL}= 4.1 mA (8.1 mA for RBC)	0		0.5	V
I_{OLC}	Output current (except RBC)	Forcing V_{OH}, V_{OL}	4			mA
I_{OLC}	Output current (RBC)	Forcing V_{OH}, V_{OL}	8			mA
I_{CC}	Supply Current (266 Mbaud)	V_{CC} = 5.25V		135	150	mA
PD	Power dissipation (266 Mbaud)	Based on I_{CC}		690		mW

Note:

1. Under both transmit and receive output switching conditions

AC Electrical Characteristics[1]

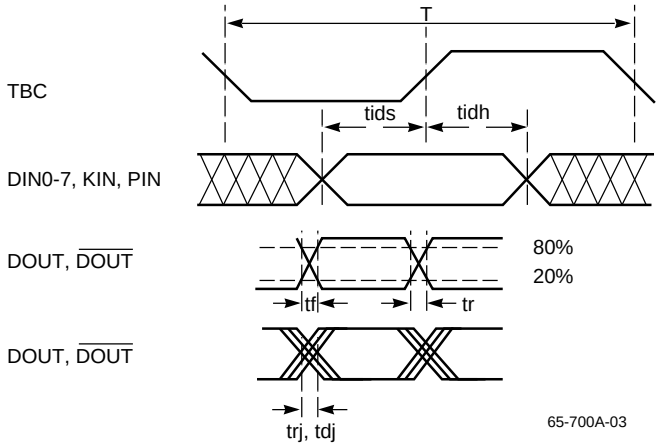
V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Transmitter						
T	TBC Period	266 Mbaud		37.7		ns
t_{acq}	Acquisition time	Note 2			1	ms
t_{ids}[6]	DIN0..7, KIN, PIN valid to TBC setup ↑		4			ns
t_{idh}[6]	TBC ↑ to DIN0..7, KIN, PIN invalid hold		4			ns
F_{out}	Output data rate		240		330	Mbaud
t_r, t_f	DOUT, $\overline{DOUT}$ rise and fall times	20% to 80% points			500	ps
t_{rj}	DOUT, $\overline{DOUT}$ pk-pk random jitter	Note 3		220		ps
t_{dj}	DOUT, $\overline{DOUT}$ pk-pk deterministic jitter	Note 4		125		ps
Receiver						
f_{cc}	Input data rate variation				±1000	ppm
D	Input data transition density to acquire and maintain lock		0.25			
t_{acq}	Loop acquisition time for 1E-12 BER				2500	bits
f_c	Loop capture range		±1000			ppm
t_j	DIN, $\overline{DIN}$ input peak to peak jitter	Note 5			0.07T	ns
t_h	RBC pulsewidth HIGH		0.4T	0.5T	0.6T	ns
t_{od}[6, 7]	RBC ↑ to DO0..7 KOUT, POUT, BSYNC delay (CSEL = 0, or CSEL = 1, POLSEL = 0)	266 Mbaud	15		25	ns
T	RBC period	266 Mbaud		37.7		ns

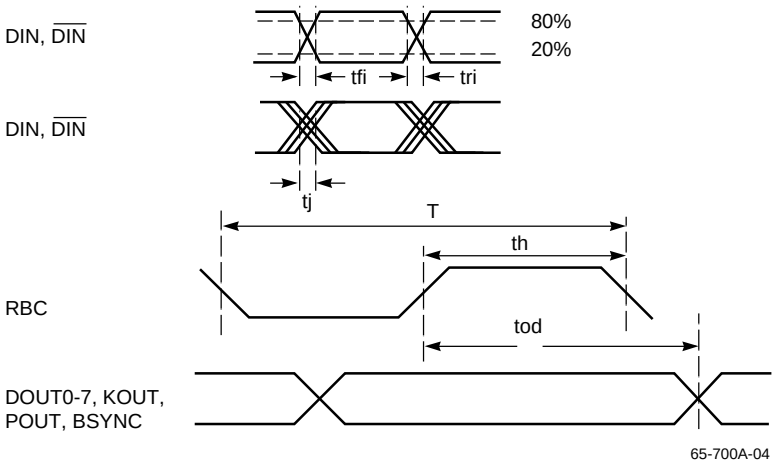
Notes:

1. Test conditions (unless otherwise indicated): PECL input rise and fall times, ≤2 ns, RLOAD = 100Ω across DOUT, $\overline{DOUT}$; TTL input rise and fall times ≤15 ns. Receiver input data rate = 265.625 Mbaud and ±1000 ppm; transition density ≥ 0.25.
2. Acquisition time is the time to establish lock once the device is powered up to the operating VCC range.
3. Input test pattern K28.7. Jitter measured at 50% amplitude, for a BER of 1E-12 with receiver running asynchronously.
4. Input test pattern K28.5. Jitter measured at 50% amplitude.
5. Guaranteed by design.
6. For CSEL = 0, the input pins are DI0..7, KIN and PIN, and the output pins are DO0..7, KOUT, and POUT. For CSEL = 1, the input pins are DI0..DI9, and the output pins are DO0..9.
7. For CSEL = 1 and POLSEL = 1, the timing specifications are with respect to the negative edge of RBC.

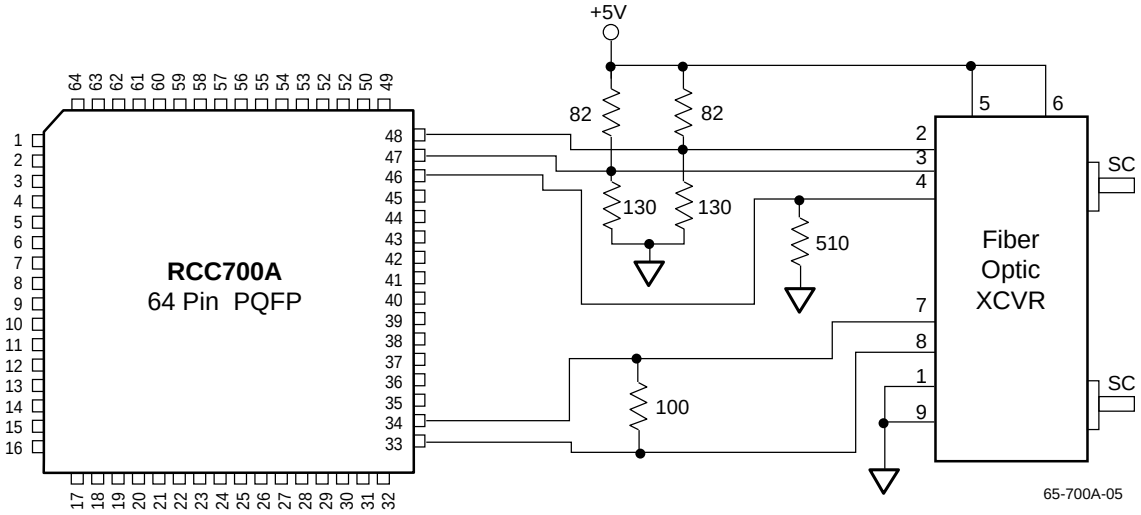
Transmitter Timing



Receiver Timing



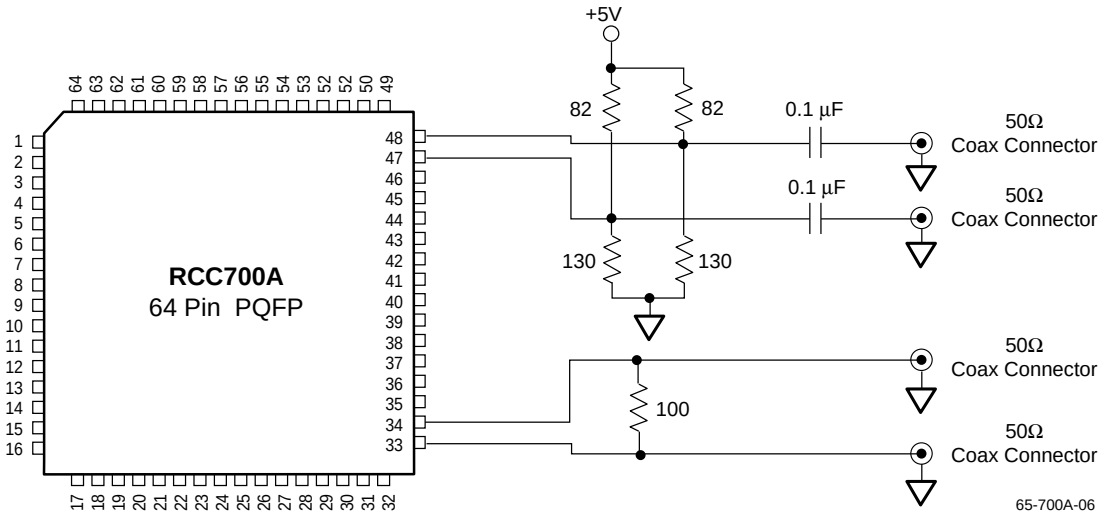
Applications Discussion



Interconnection of RCC700A to a Fiber Optic Transceiver

Recommended Fiber Optic Transceivers:

1. HP BR-5302
2. Siemens V23806-A7-C2



Interconnection of RCC700A to a Coax Cable

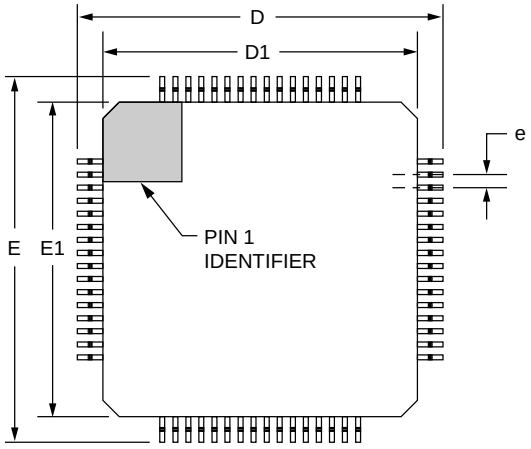
Mechanical Dimensions

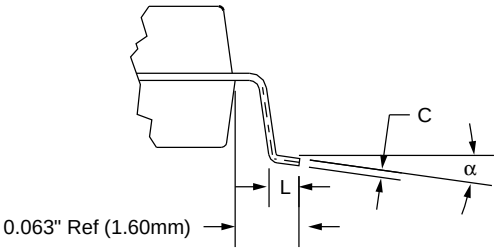
64-Lead MQFP Package

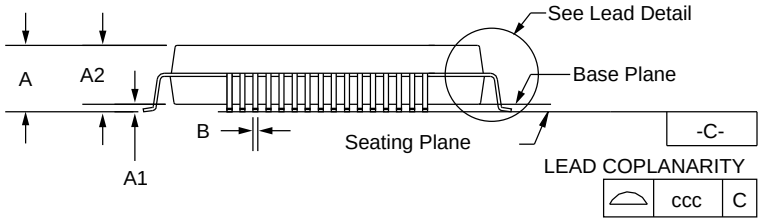
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.096	—	2.45	
A1	.010	—	.25	—	
A2	.077	.083	1.95	2.10	
B	.007	.011	.17	.27	7
D/E	.510	.530	12.95	13.45	
D1/E1	.390	.398	9.90	10.10	2
e	.020 BSC		.50 BSC		
L	.031	.040	.78	1.03	6
N	64		64		4
ND	16		16		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.







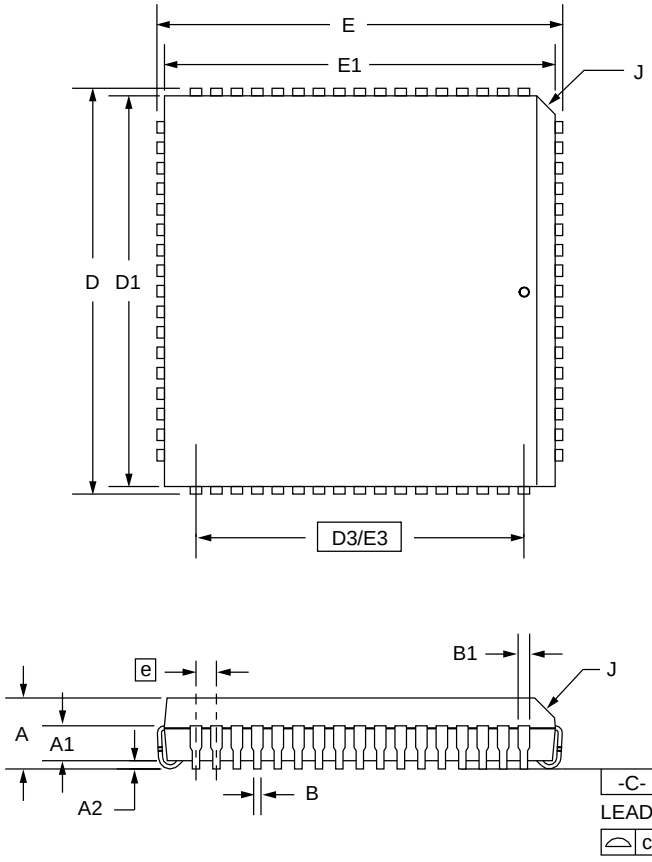
Mechanical Dimensions (continued)

68-Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.985	.995	25.02	25.27	
D1/E1	.950	.958	24.13	24.33	3
D3/E3	.800 BSC		20.32 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	17		17		
N	68		68		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Part Number	Package
RCC700AKA	64 PQFP
RCC700AQD	68 PLCC

Raytheon Electronics
Semiconductor Division
350 Ellis Street
Mountain View CA 94043
415 968 9211
FAX 415 966 7742